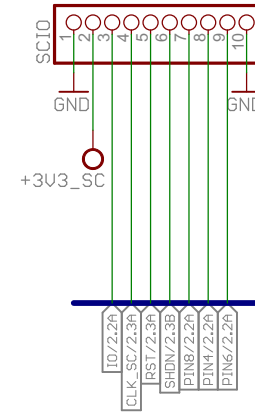
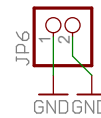
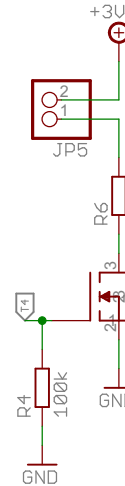
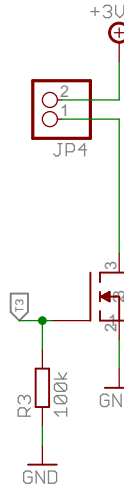
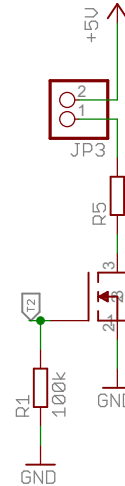
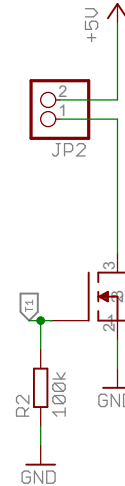
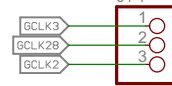
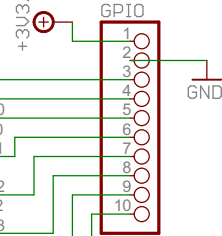


USB FPGA MODULE 1.11 (CDF-FPGA)

C3~R16~IO_L49N_M1DQ11_1
D8~K16~IO_L44N_A2_M1DQ7_1
D9~L16~IO_L47N_LDC_M1DQ1_1
D10~M16~IO_L46N_FOE_B_M1DQ3_1
F10~N16~IO_L45N_A0_M1LDQSN_1
D11~P16~IO_L48N_M1DQ9_1
F11~M15~IO_L46P_FCS_B_M1DQ2_1
D12~P15~IO_L48P_HDC_M1DQ8_1
F12~R15~IO_L49P_M1DQ10_1
D13~T15~IO_L50N_M1UDQSN_1
F13~L14~IO_L47P_FWE_B_M1DQ0_1
D14~K15~IO_L44P_A3_M1DQ6_1
F14~N14~IO_L45P_A1_M1LDQS_1
D15~R14~IO_L50P_M1UDQS_1
F15~L13~IO_L53N_VREF_1
D16~M13~IO_L74P_AWAKE_1
F16~L12~IO_L53P_1
D17~M12~IO_L2P_CMPCLK_2
F17~R12~IO_L52P_M1DQ14_1
F18~M11~IO_L2N_CMPMOSI_2
D19~T12~IO_L16P_2
F19~M10~IO_L16N_VREF_2
C20~P8~IO_L30P_GCLK1_D13_2
D20~R9~IO_L23P_2
F20~T9~IO_L23N_2
C21~M9~IO_L29P_GCLK3_2
D21~N9~IO_L14P_D11_2
F21~P9~IO_L14N_D12_2
C22~T7~IO_L32N_GCLK28_2
D22~N8~IO_L29N_GCLK2_2
F22~T8~IO_L30N_GCLK0_USERCCLK_2
C23~M7~IO_L31N_GCLK30_D15_2
D23~P7~IO_L31P_GCLK31_D14_2
F23~R7~IO_L32P_GCLK29_2
C24~N6~IO_L64N_D9_2
D24~P6~IO_L47P_2
F24~T6~IO_L47N_2
C25~M6~IO_L64P_D8_2
D25~P4~IO_L63P_2
F25~T4~IO_L63N_2

CON1_CDF-FPGA



TODD: Clock glitching output and/or maybe analog mux?

Analog mux useful if we only have 3.3 / 5 / GND (no ext supply)

David Oswald

board

23.09.2019 13:54:06

Sheet: 3/3